Date

2/19/2018

# Stage proposal (HW)

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|        | Date      | Rev   |  |  |  |  |
|--------|-----------|-------|--|--|--|--|
| nastro | 2/19/2018 | V0.01 |  |  |  |  |

## 1 Revision History

| Rev   | Date       | Prepared by  | Changes Made                |
|-------|------------|--------------|-----------------------------|
| V0.01 | 05/12/2017 | P. Delmastro | First Issue of the document |

### 2 General

DAC System is a young company based in Manno (TI), active in the Broadcast industry. In the last three years we have been developing and marketing our patented system: DACS (Direct Antenna Control System).

The system is designed to monitor, in-service and in real time, the health of high power transmission systems, typical of broadcast transmissions (DVB-T, DAB, FM Radio).

DAC System is open to host students in its structure to implement small development projects in cooperation with internal R&D. In this document one of the opportunities will be described.

### 3 **Project Description: Redesign of ASIB Board**

The object of the stage is the implementation of changes in the existing design of an acquisition system called "Junction Box", part of DACS System. The current design must be modified for three reasons:

- Improve the surge protection capability of the interface of the so called Motherboard, by means of properly dimensioned GDT (Gas Discharge Tubes) and PTC Thermistors
- Add a configuration option by means of SMD jumpers on the so called AISB Board.
- Migrate the design from Cadence Allegro environment to the tool that will be selected by DAC System as standard development tool.

Although the changes have low complexity, the task is not trivial because of the third bullet.

# 4 Technology

The existing design is available in Cadence Allegro format. DAC System is currently utilizing an open source tool for PCB development and is evaluating the opportunity to migrate to a professional commercial solution.

In any case, it will be most probably needed a migration work, to the target development environment.



The boards to be reworked have low to medium complexity, both built on 4 layers FR4, with analog and digital signals (Motherboard) or only analog signals (ASIB), main DC supply: 48V.

#### 5 Expected competences

The student will be expected to have followed an electronic engineering study address. Specifically, the following skills will be required and exercised during the stage:

- Knowledge of PCB development practices and of one development environment
- Practical experience of board schematic entry
- Practical experience of PCB layout design
- Fluent writing and reading in English
- Some experience with common electronics lab tools (oscilloscopes, debuggers)

#### 6 Tasks included in the assignment

The contents of the stage assignment can be agreed. One or both the boards can be subject of the assignment.

Minimum Duration: 2 months

Preferred Duration: 4 months

Expected start: Any time